The ADC and LVD Measurements in GPL833F08A

INTRODUCTION AND ANALYSIS

In GPL833F08A, we suggest the following ways for ADC and LVD functions:

A. For ADC Function, connect an I/O pin (any pin from PB[7:0]) and VREG pin for voltage reference (1.8V).

B. For LVD (Low Voltage Detection) function, implement it with the ADC approach.

SUGGESTION

The way we use ADC to detect voltage in GPL833F08A:

1. Connect one ADC channel (PB0~7) to Vreg pin, i.e. using Vreg 1.8V for reference voltage, and suppose 0xaaa is obtained. Another ADC channel is connected to the position where is under measured. The voltage should be “1.8V * (0xbbb/0xaaa)” if 0xbbb is obtained.
2. Implement LVD (Low Voltage Detection) using ADC approach: Connect the battery power to VDD_ADC pin. Measure the ADC from Vreg. Suppose we get 0xaaa and it is the voltage reference for 1.8V. Next, measure ADC VBAT channel (0x3341[3:0] = 1010, and 0x3341.b5 = 1). The ADC data is 1/5VDD_ADC. If 0xbbb is obtained, the battery voltage = 5 * (0xbbb / 0xaaa) *1.8.
3. Because enabling ADC consumes more power, we recommend ADC retaining disabled while ADC is not detecting voltage. In order to use ADC channel IO(PB0~PB7), the corresponding setting to 0x3086 register should be properly given, i.e. setting the IO to line-in function.

EXAMPLE CODE

Step1: Set ADC enable and select channel

```
LDA     #D_ADCEn+ D_ADCPB0
STA     P_ADC_Ctrl2
```

Step2: Set ADC voltage reference

```
LDA     #D_ADCVregVDD+ D_ADCVregEn
STA     P_ADC_VREF_Ctrl
```

Step3: Set ADC clock, sample and hold cycle, trigger mode and ADC start

```
LDA     #D_ADCClkDiv2 8+ D_ADCSHCycle16 + D_ADCTrigManual + D_ADCStart
STA     P_ADC_Ctrl1
```

Step4: Read ADC status (interrupt flag) and determine whether or not ADC conversion is ready

```
L_Ready?:
```

```
%WatchDogClear
LDA     P_ADC_Ctrl2
AND     #D_ADCStatus
BEQ     ?L_Ready
```

Step5: Get ADC data

```
LDA     P_ADC_Data_LB
STA     R_ADC_LB
LDA     P_ADC_Data_HB
STA     R_ADC_HB
```

Step6: Stop ADC function or set another channel, get ADC data